

Claims

What is claimed is:

Claim 1

- 1 1. A control system, comprising:
2 a storage device to store data signals;
3 a circuit coupled to the storage device to receive as control signals
4 predetermined ones of the data signals, the control signals to control operation
5 of the circuit when the circuit is operating in a first mode; and
6 Error Correction Code (ECC) logic coupled to the storage device to
7 interpret the predetermined ones of the data signals as ECC check bits to detect
8 errors in the data signals when the circuit is operating in a second mode.

Claim 2

- 1 2. The system of Claim 1, wherein the storage device is a memory having
2 multiple addressable storage locations, each storing a different respective set of
3 data signals.

Claim 3

- 1 3. The system of Claim 2, wherein each of the addressable storage locations
2 includes circuits to store a respective mode designator to control whether the
3 circuit operates in the first or the second mode after the data signals stored at
4 the addressable storage location are read from the memory.

Claim 4

- 1 4. The system of Claim 3, wherein the circuit includes branch logic to utilize
2 the predetermined ones of the data signals stored at an addressable storage
3 location to generate a next address for addressing the memory if the mode
4 designator stored at the addressable storage location indicates the circuit will
5 operate in the first mode.

Claim 5

- 1 5. The system of Claim 1, wherein the storage device includes storage
2 circuits to store a mode designator, the mode designator to control whether the
3 circuit will operate in the first or the second mode.

Claim 6

- 1 6. The system of Claim 1, wherein the circuit includes logic to provide one or
2 more functions of an instruction processor.

Claim 7

- 1 7. The system of Claim 1, and further including a programmable storage
2 device coupled to the circuit to select the predetermined ones of the data
3 signals.

Claim 8

- 1 8. The system of Claim 1, and further including at least one parity circuit
2 coupled to the storage device to determine whether a parity error occurred on
3 any of a predetermined set of the data signals.

Claim 9

- 1 9. The system of Claim 8, wherein the at least one parity circuit includes a
2 circuit to determine whether a parity error occurred on the predetermined set of
3 the data signals when the circuit is operating in the second mode.

Claim 10

- 1 10. The system of Claim 1, wherein the ECC logic is coupled to ECC
2 complement logic to correct errors in the data signals that are detected by the
3 ECC logic when operating in the second mode.

Claim 11

- 1 11. The system of Claim 10, and further including logic coupled to the ECC
2 complement logic to provide the data signals to the circuit for use as control
3 signals after any errors detected by the ECC logic have been corrected.

Claim 12

- 1 12. A method of controlling a digital system, comprising:
2 a.) reading first data signals from a storage device;
3 b.) interpreting the first data signals as control signals to control one or
4 more functions of the digital system if operating in a first mode of operation; and
5 c.) interpreting the first data signals as Error Correction Code (ECC)
6 signals if operating in a second mode of operation.

Claim 13

- 1 13. The method of Claim 12, and further including:
2 reading second data signals from the storage device; and
3 using the ECC signals to detect errors in the second data signals if
4 operating in the second mode of operation.

Claim 14

- 1 14. The method of Claim 13, wherein the storage device is a memory, and
2 wherein the first and second data signals are stored at a same addressable
3 location within the memory.

Claim 15

- 1 15. The method of Claim 14, wherein multiple memory addresses each stores
2 different respective first and second data signals.

Claim 16

- 1 16. The method of Claim 15, and further including using the first data signals
2 to generate a next address for addressing the memory when operating in the first
3 mode of operation.

Claim 17

- 1 17. The method of Claim 15, and further including:
2 reading one of the multiple memory addresses; and
3 interpreting at least one of the second data signals as a mode indicator to
4 indicate whether operation is occurring in the first or the second mode of
5 operation.

Claim 18

- 1 18. The method of Claim 17, and including repeating the steps of Claim 17 for
2 multiple memory addresses.

Claim 19

- 1 19. The method of Claim 13, and further including, correcting an error if the
2 error is detected in predetermined ones of the second data signals.

Claim 20

- 1 20. The method of Claim 19, and further including programmably selecting
2 the predetermined ones of the second data signals.

Claim 21

- 1 21. The method of Claim 12, and further including programmably selecting
2 the first data signals.

Claim 22

- 1 22. The method of Claim 13, and further including interpreting one or more of
2 the second data signals as control signals to control an arithmetic logic unit of an
3 instruction processor.

Claim 23

- 1 23. The method of Claim 13, and further including using parity bits to detect a
2 parity error occurring within the first or the second data signals.

Claim 24

- 1 24. The method of Claim 23, and further including:
2 reporting any error detected using the ECC signals; and
3 reporting any error detected using the parity bits.

Claim 25

- 1 25. The method of Claim 24, and further including:
2 servicing any error detected by the ECC signals at a time that is optimal
3 for the digital system; and
4 servicing any error detected using the parity bits substantially
5 immediately.

Claim 26

- 1 26. A control system having a first and second mode of operation,
2 comprising:
3 storage means for storing data signals;

4 control means for utilizing first ones of the data signals to affect
5 operations of the control system when operating in the first mode; and
6 error means for interpreting the first ones of the data signals as check bits
7 for detecting errors occurring in second ones of the data signals when the
8 control system is operating in the second mode.

Claim 27

1 27. The system of Claim 26, wherein the storage means includes means for
2 storing a mode designator to control whether the control system is operating in
3 the first or the second mode.

Claim 28

1 28. The system of Claim 26, wherein the control means includes branch
2 means for utilizing the first ones of the data signals to generate an address for
3 the storage means.

Claim 29

1 29. The system of Claim 26, wherein the storage means is a memory
2 including predetermined addressable locations, each storing a different
3 respective set of the first and second ones of the data signals.

Claim 30

1 30. The system of Claim 29, wherein each of the predetermined addressable
2 locations within the memory includes means for storing a mode designator for
3 controlling whether the control system operates in the first or the second mode
4 when the first and the second ones of the data signals stored at the addressable
5 location are read from the memory.

Claim 31

- 1 31. The system of Claim 30, wherein the error means includes means for
2 correcting an error detected on predetermined ones of the second ones of the
3 data signals when the control system is operating in the second mode.

Claim 32

- 1 32. The system of Claim 31, and further including means for providing
2 corrected ones of the second ones of the data signals to the control means for
3 use in affecting the operations of the control system.

Claim 33

- 1 33. The system of Claim 31, and further including parity detection means for
2 detecting parity errors within the first or the second ones of the data signals.

Claim 34

- 1 34. The system of Claim 33, wherein the parity detection means includes
2 means for detecting uncorrected parity errors remaining within the second ones
3 of the data signals.

Claim 35

- 1 35. The system of Claim 33, and further including maintenance means for
2 performing error recovery actions within a first time period for errors detected by
3 the parity detection means and, for errors detected by the error means,
4 performing error recovery actions any time the control system is appropriately
5 configured.

Claim 36

- 1 36. The system of Claim 26, and further including means for programmably
2 selecting the first ones of the data signals.

Claim 37

- 1 37. The system of Claim 31, and further including means for programmably
- 2 selecting the predetermined ones of the second ones of the data signals.